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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,913	CARLSON, ROY M.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *48-55* is/are allowed.

6)☒ Claim(s) *1-8,16-20,23,25-27,32,33,40,41,44,45 and 56-60* is/are rejected.

7)☒ Claim(s) *9-15,21-22,24,28-31,34-39,42,43,46 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/05,9/05*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 9-27-2005 has been entered.

Claim Objections

Claims 3, 6, 19, 21, 25, 36 and 40 are objected to because of the following informalities:

"an radiation-particle " on line 2 of claims 3 and 6 appears to be --a radiation-particle --;

"second gates" on line 1 and 3-4 of claim 25 appears to be --second logic gates--;

"each the first and second gates" on line 2 of claims 19 and 36 appears to be --each of the first and second logic gates--;

"first gate" on line 4 and "second gate" on line 5 of claim 21 appears to be --first logic gate-- and --second logic gate-- respectively; and

"one logic" on line 2 of claim 40 appears to be --one logic gate--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 19-20, 23, 32-33, 40-41, 44-45 and 56-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Knowles (US 2002/0175713 A1).

Regarding claim 1, Fig. 1 of Knowles teaches a system for hardening a logic circuit against at least one of a single-event upset and single-event transient condition (col. 1, lines 64-67), the system comprising in combination: a logic circuit (pass gate coupled to D and CK) outputting independently-obtained first and second redundant signals (output signals of the pass gates are independently obtained by CK signal); first and second feed-forward devices (first set of dual port inverters comprising a PMOS and a NMOS being coupled to the output of the pass gate), wherein each of the first and second feed-forward devices is operable to receive both of the first and second redundant signals (gates of PMOS and NMOS receives the output signal of the pass gate), and wherein when the first and second redundant signals are in expected states, then (i) the first feed-forward device responsively provides a first feed-forward signal and (ii) the second feed-forward device responsively provides a second feed-forward signal (when the outputs of the pass gate are the same, i.e. "expected state", the dual

port inverters provides output signals respectively); and first and second feedback devices (the second set of dual port inverters coupled to the first set of dual port inverters), wherein each of the first and second feedback devices is operable to receive both of the first and second feed-forward signals (the second set of dual port inverters receives the output of the first set of dual port inverters), and wherein when the first and second feed-forward signals are in expected states (when the outputs of the first set of dual port inverters are the same, i.e. "expected states", the second set of dual port inverters provides the output signals), (i) the first feedback device responsively feeds a first feedback signal back to the first redundant signal and (ii) the second feedback device responsively feeds a second feedback signal back to the second redundant signal (the output signals of the second set of dual port inverters are feedback to the output of the pass gates respectively).

Regarding claim 2, Fig. 1 of Knowles teaches the system of claim 1, wherein when at least one of the first and second redundant signals is in an unexpected state (when the outputs of pass gates are not the same due to the single event upset, i.e. "unexpected state), then at least one of the first and second feed-forward devices continues to provide its respective feed-forward signal consistent with the last expected state of the redundant signals (the latch comprising the first and second dual port inverters keeps the previous state as a result of parasitic capacitance present at the output of the inverters; col. 5, lines 36-45).

Regarding claim 3, Fig. 1 of Knowles teaches the system of claim 2, wherein at least one of the first and second redundant signals is in the unexpected state as a result of a radiation-particle intrusion (col. 1, lines 15-24).

Regarding claim 4, Fig. 1 of Knowles teaches the system of claim 2, wherein the unexpected state is propagated by any of the logic circuit, the first and second redundant signals, and the first and second feedback modules (single event upset is random and happens in any signal path of a circuit; col. 1, lines 16-34).

Regarding claim 5, Fig. 1 of Knowles teaches the system of claim 1, wherein when at least one of the first and second feed-forward signals is in an unexpected state, then at least one of the first and second feedback devices continues to provide its respective feedback signal consistent with the last expected state of the feed-forward signals (the latch comprising the first and second dual port inverters keeps the previous state as a result of parasitic capacitance present at the output of the inverters; col. 5, lines 36-45).

Regarding claim 6, Fig. 1 of Knowles teaches the system of claim 5, wherein at least one of the first and second feed-forward signal is in the unexpected state as a result of a radiation-particle intrusion (col. 1, lines 15-24).

Regarding claim 7, Fig. 1 of Knowles teaches the system of claim 5, wherein the unexpected state occurs in any of the logic circuit, the first and second redundant signals, the first and second feed-forward modules, and the first and second feed-forward signals (any part of the circuit is subject to the single event upset, SEU, in outer space or orbital environment; col. 1, lines 16-24).

Regarding claim 8, Fig. 1 of Knowles teaches the system of claim 1, wherein any of the logic circuit, first and second feed-forward devices, and first and second feedback devices comprise radiation-particle-hardened circuitry (Fig. 1 uses state-restoring feedback paths to minimize SEU susceptibility which makes the circuit being radiation-particle hardened).

Regarding claim 19, Fig. 1 of Knowles teaches the system of claim 1, wherein the logic circuit comprises first and second logic gates, wherein each the first and second gates (two pass gates receive the input signal D and produce an output respectively) has (i) at least one input for receiving a desired input signal and (ii) an output for producing its redundant signal.

Regarding claim 20, Fig. 1 of Knowles teaches the system of claim 19, wherein the first and second logic gates comprise radiation-particle-hardened circuitry (Fig. 1 uses state-restoring feedback paths to minimize SEU susceptibility and the circuitry of

Fig. 1 being radiation-particle hardened where the first and second pass gate is a part of the radiation-particle-hardened circuitry).

Regarding claim 23, Fig. 1 of Knowles teaches the system of claim 19, wherein each of the first and second gates further include at least one input for receiving an enable signal (CK being enable signal), and wherein the enable signal allows each of the first and second gates to provide a current state of its respective redundant signal (when CK is high, the pass gates provide the current state of the input signal to the pass gate which is the redundant signal).

Regarding claim 32, Fig. 1 of Knowles teaches the system of claim 1, wherein the first feed-forward device comprises at least one logic gate (the dual port inverter comprising PMOS and NMOS acts as an inverter logic gate having two inputs and one output), wherein the at least one logic gate has (i) at least two inputs, and (ii) an output for producing its feed forward signal, wherein one of the inputs is operable to receive the first redundant signal, and wherein another of the inputs is operable to receive the second redundant signal (PMOS receives the output signal from a first pass gate while the NMOS receives the output signal from the second pass gate).

Regarding claim 33, Fig. 1 of Knowles teaches the system of claim 32, wherein the at least one logic gate comprises radiation-particle-hardened circuitry (Fig. 1 uses state-restoring feedback paths to minimize SEU susceptibility and the circuitry of Fig. 1

being radiation-particle hardened where the first and second pass gate is a part of the radiation-particle-hardened circuitry).

Regarding claim 40, Fig. 1 of Knowles teaches the system of claim 1, wherein the first feedback device (dual port inverter circuit outputting Q) comprises at least one logic gate (dual port inverter is an inverter logic gate having two inputs and one output), wherein the at least one logic has (i) at least two inputs, and (ii) an output for producing its feedback signal (the output Q is feedback to the output of the pass gate which is a redundant signal), wherein one of the inputs is operable to receive the first feed-forward signal (PMOS receives the output of first dual port inverter while the NMOS receives the output of the second dual port inverter), and wherein another of the inputs is operable to receive the second feed-forward signal.

Regarding claim 41, Fig. 1 of Knowles teaches the system of claim 40, wherein the at least one logic gate comprises radiation-particle-hardened circuitry (Fig. 1 uses state-restoring feedback paths to minimize SEU susceptibility and the circuitry of Fig. 1 being radiation-particle hardened where the dual port inverter is a part of the radiation-particle-hardened circuitry).

Regarding claim 44, Fig. 1 of Knowles teaches the system of claim 1, wherein the second feedback device (dual port inverter circuit outputting /Q) comprises at least one logic gate (dual port inverter is an inverter logic gate having two inputs and one

output), wherein the at least one logic gate has (i) at least two inputs, and (ii) an output for producing its feedback signal (the output /Q is feedback to the output of the pass gate which is a redundant signal), wherein one of the inputs is operable to receive the first feed-forward signal (PMOS receives the output of second dual port inverter while the NMOS receives the output of the first dual port inverter), and wherein another of the inputs is operable to receive the second feed-forward signal.

Regarding claim 45, Fig. 1 of Knowles teaches the system of claim 40, wherein the at least one logic gate comprises radiation-particle-hardened circuitry (Fig. 1 uses state-restoring feedback paths to minimize SEU susceptibility and the circuitry of Fig. 1 being radiation-particle hardened where the dual port inverter is a part of the radiation-particle-hardened circuitry).

Regarding the method claims 56-60 are essentially the same scope as the apparatus claims 1-9, where a single event upset hardened latch circuit of Knowles shown in Fig. 1 teaches the method for hardening a logic circuit against at least one of a single event upset and single event transient condition when any of the redundant signals, the feed-forward signals and the feedback signals are in either expected state, i.e. the same logic level, or unexpected state, e.g. the different logic level due to the single event upset condition where the logic operation is operable to not change a current state by putting the circuit in a floating state and maintaining the previous state

as a result of parasitic or stray capacitance (col. 5, lines 34-46), and thus claims 56-60 are rejected similarly.

Claims 1-8, 19-20, 23, 25-27, 32-33, 40-41, 44-45 and 56-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (US PAT No. 6,327,176).

Regarding claim 1, Fig. 4 of Li et al. teaches a system for hardening a logic circuit against at least one of a single-event upset and single-event transient condition (col. 1, lines 10-15), the system comprising in combination: a logic circuit (pass gates 46 and 47) outputting independently-obtained first and second redundant signals (output signals of the pass gates are independently obtained by C and /C signals); first and second feed-forward devices (two dual port inverters in 44), wherein each of the first and second feed-forward devices is operable to receive both of the first and second redundant signals (gates of P1 and N1 receives the output signal of the pass gate), and wherein when the first and second redundant signals are in expected states, then (i) the first feed-forward device (P1/ N1) responsively provides a first feed-forward signal (the output of 46) and (ii) the second feed-forward device (P2 / N2) responsively provides a second feed-forward signal (when the outputs of 46 and 47 are the same, i.e. "expected state", P1/N1 provides output signals respectively); and first and second feedback devices (P1'/N1' and P2'/N2' in 45), wherein each of the first (P1'/N1') and second (P2'/N2') feedback devices is operable to receive both of the first and second feed-forward signals (P1' receives the output of P1/N1 and N1 receives the output of P2/N2), and wherein when the first and second feed-forward signals are in expected states

(when the outputs of P1/N1 and P2/N2 are the same, i.e. "expected states", 45 provides the output signals), (i) the first feedback device responsively feeds a first feedback signal back to the first redundant signal (output of P1'/N1' feedback to the output of 46 via 48)and (ii) the second feedback device responsively feeds a second feedback signal back to the second redundant signal (the output signals of P2'/N2' feedback to the output of 47).

Regarding claim 2, Fig. 4 of Li et al. teaches the system of claim 1, wherein when at least one of the first and second redundant signals is in an unexpected state (when the outputs of 46, 47 are not the same due to the single event upset, i.e. "unexpected state), then at least one of the first and second feed-forward devices continues to provide its respective feed-forward signal consistent with the last expected state of the redundant signals (dual gate inverters in 44 comprising P1/N1 and P2/N2 keeps the previous state as a result of parasitic capacitance present at the output of P1/N1 and P2/N2 when the input signal to the gate of P1/N1 and P2/N2 are different, i.e. unexpected state since P1/N1 or P2/N2 becomes a floating state).

Regarding claim 3, Fig. 4 of Li et al. teaches the system of claim 2, wherein at least one of the first and second redundant signals is in the unexpected state as a result of a radiation-particle intrusion (col. 3, lines 1-3).

Regarding claim 4, Fig. 4 of Li et al. teaches the system of claim 2, wherein the unexpected state is propagated by any of the logic circuit, the first and second redundant signals, and the first and second feedback modules (single event upset is random and happens in any signal path of a circuit; col. 1, lines 24-34).

Regarding claim 5, Fig. 4 of Li et al. teaches the system of claim 1, wherein when at least one of the first and second feed-forward signals is in an unexpected state, then at least one of the first and second feedback devices continues to provide its respective feedback signal consistent with the last expected state of the feed-forward signals (dual gate inverters in 45 comprising P1'/N1' and P2'/N2' keeps the previous state as a result of parasitic capacitance present at the output of P1'/N1' and P2'/N2' when the input signal to the gate of P1'/N1' and P2'/N2' are different, i.e. unexpected state sinceP1'/N1' or P2'/N2' becomes a floating state).).

Regarding claim 6, Fig. 4 of Li et al. teaches the system of claim 5, wherein at least one of the first and second feed-forward signal is in the unexpected state as a result of a radiation-particle intrusion modules (single event upset is random and happens in any signal path of a circuit; col. 1, lines 24-34).

Regarding claim 7, Fig. 4 of Li et al. teaches the system of claim 5, wherein the unexpected state occurs in any of the logic circuit, the first and second redundant signals, the first and second feed-forward modules, and the first and second feed-

forward signals modules (single event upset is random and happens in any signal path of a circuit; col. 1, lines 24-34).

Regarding claim 8, Fig. 4 of Li et al. teaches the system of claim 1, wherein any of the logic circuit, first and second feed-forward devices, and first and second feedback devices comprise radiation-particle-hardened circuitry (col. 1, lines 46-55).

Regarding claim 19, Fig. 4 of Li et al. teaches the system of claim 1, wherein the logic circuit comprises first and second logic gates (46 and 47) wherein each of the first and second logic gates (46 comprising pass gates P7/N7 receive the input signal 41 and produce an output, and 47 comprising pass gates P8/N8 receive the input signal 41 and produce an output) has (i) at least one input for receiving a desired input signal (46 and 47 receive input signal 41) and (ii) an output for producing its redundant signal (output of 46 and 47).

Regarding claim 20, Fig. 4 of Li et al. teaches the system of claim 19, wherein the first and second logic gates comprise radiation-particle-hardened circuitry (Fig. 4 being radiation-particle hardened where the first and second pass gate 46, 47 are a part of the radiation-particle-hardened circuitry).

Regarding claim 23, Fig. 4 of Li et al. teaches the system of claim 19, wherein each of the first and second gates further include at least one input for receiving an

enable signal (C being enable signal), and wherein the enable signal allows each of the first and second gates to provide a current state of its respective redundant signal (when C is high, 46 and 47 provide the current state of the input signal at the output of 46 and 47 which is the redundant signal).

Regarding claim 25, Fig. 4 of Li et al. teaches the system of claim 19, wherein each of the first and second logic gates further include at least two inputs (46 has two input gates of P7 and N7 receiving enabling signals C and /C respectively) for receiving enable and complementary signals (C and /C), and wherein the enable and complementary signals allow each of the first and second logic gates to provide a current state of its respective redundant signal (based on C and /C, the 46 provides the redundant signal to 44 and the 47 provides the redundant signal to 44).

Regarding claim 26, Fig. 4 of Li et al. teaches the system of claim 25 wherein the current state of the respective redundant signals comprises any of a high state, a low state, and a floating state (when C is logic high, P7 and N7 (P8/ N8) are enabled and provides the redundant signals, logic high or logic low based on the input signal at 41 while the output of 46 (47) floats when C is logic low since P7 and N7 (P8/N8) are disabled).

Regarding claim 27, Fig. 4 of Li et al. teaches the system of claim 25, further including a clocking circuit to provide the enable and complementary signals (signal C and /C inherently requires a clock circuit producing signals C and /C).

Regarding claim 32, Fig. 4 of Li et al. teaches the system of claim 1, wherein the first feed-forward device comprises at least one logic gate (the dual port inverter comprising PMOS P1 and NMOS N1 acts as an inverter logic gate having two inputs and one output), wherein the at least one logic gate has (i) at least two inputs(gate of P1 and gate of N1) and (ii) an output (output at the common node of P1 and N1 for producing its feed forward signal, wherein one of the inputs is operable to receive the first redundant signal (P1 receives the output of 47), and wherein another of the inputs is operable to receive the second redundant signal (N1 receives the output of 46).

Regarding claim 33, Fig. 4 of Li et al. teaches the system of claim 32, wherein the at least one logic gate comprises radiation-particle-hardened circuitry (Fig. 4 being radiation-particle hardened where the first and second pass gate is a part of the radiation-particle-hardened circuitry).

Regarding claim 40, Fig. 4 of Li et al. teaches the system of claim 1, wherein the first feedback device (dual port inverter circuit comprising P1'/N1') comprises at least one logic gate (two gate inputs and one output), wherein the at least one logic gate has (i) at least two inputs (gates of P1' and N1'), and (ii) an output for producing its feedback

signal (the output of P1' and N1' is feedback to the output of 46 via 48), wherein one of the inputs is operable to receive the first feed-forward signal (P1' receives the output of P1/N1), and wherein another of the inputs is operable to receive the second feed-forward signal (N1' receives the output of P2/N2).

Regarding claim 41, Fig. 4 of Li et al. teaches the system of claim 40, wherein the at least one logic gate comprises radiation-particle-hardened circuitry (Fig. 4 being radiation-particle hardened where the dual port inverter is a part of the radiation-particle-hardened circuitry).

Regarding claim 44, Fig. 4 of Li et al. teaches the system of claim 1, wherein the second feedback device (dual port inverter circuit comprising P2'/N2') comprises at least one logic gate (P2'/N2' having two gate inputs and one output), wherein the at least one logic gate has (i) at least two inputs (gates of P2'/N2'), and (ii) an output for producing its feedback signal (the output of P2'/N2' feedback to the output of 47 via 49), wherein one of the inputs is operable to receive the first feed-forward signal (P2' receives the output of P2/N2), and wherein another of the inputs is operable to receive the second feed-forward signal (N2' receives the output of P1/N1).

Regarding claim 45, Fig. 4 of Li et al. teaches the system of claim 40, wherein the at least one logic gate comprises radiation-particle-hardened circuitry (Fig. 4 being

radiation-particle hardened where the dual port inverter is a part of the radiation-particle-hardened circuitry).

Regarding the method claims 56-60 are essentially the same scope as the apparatus claims 1-8, where a single event upset hardened latch circuit of Li et al. shown in Fig. 4 teaches the method for hardening a logic circuit against at least one of a single event upset and single event transient condition when any of the redundant signals, the feed-forward signals and the feedback signals are in either expected state, i.e. the same logic level, or unexpected state, e.g. the different logic level due to the single event upset condition where the logic operation is operable to not change a current state by putting the circuit in a floating state and maintaining the previous state as a result of inherent parasitic or stray capacitance, and thus claims 56-60 are rejected similarly.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knowles and Li et al.

Regarding claim 16-18, Fig. 1 of Knowles and Fig. 4 of Li et al. teaches the system according to claim 1, but does not teach the logic circuit, first and second feed-forward devices and first and second feedback devices being fabricated using a bulk silicon, a device insulating, or a silicon-on-insulting technologies. However, Knowles teaches the utilization of the silicon-on-insulator processes, i.e. the device insulating technology and the use of large-area device, so called bulk silicon technology for the purpose of providing reducing or minimizing SEU(Single Event Upset) susceptibility in the description of the background art (paragraph [0006] and [0007]). It would have been obvious at the time of invention to utilize the various transistor manufacturing technologies, e.g. a bulk silicon, a device insulating, or a silicon-on-insulting technologies as described in the specification of Knowles since it would provide reduction of SEU susceptibility.

Allowable Subject Matter

Claims 48-55 are allowable over the prior art of record.

Claims 9-15, 21-22, 24, 28-31, 34-39, 42-43, and 46-47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Knowles and Li et al. teaches single event upset hardened latch circuit, one of ordinary skill in the art would not have been motivated to modify the teaching of Knowles and/or Li et al. to further includes, among other things, the specific

of the first and second feed-forward device providing a current sate of their respective first and second feed-forward signals in response to enable signals (claims 9, 13), the logic circuit being fabricated according to a tri-rail system where the first gate formed between the first adjacent rail and the common rail (claim 21), the second clocking module providing the second logic gate independently-oriented second enable and complementary signals (claim 28), a tri-rail system where at least one logic gate of the first feed-forward device is formed between the first adjacent rail and the common rail (claim 34) or between the second adjacent rail and common rail (claim 35), the second feed-forward device having each of the first and second logic gates having two input where one input receives the first redundant signal and another input receives the second redundant signal (claim 36), a tri-rail system where at least one logic gate of the first feedback device is formed between the first adjacent rail and the common rail (claim 42) or between the second adjacent rail and common rail (claim 43), a tri-rail system where at least one logic gate of the second feed-forward device is formed between the first adjacent rail and the common rail (claim 46) or between the second adjacent rail and common rail (claim 47).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H Cho

James H. Cho
Primary Examiner
Art Unit 2819

Date: 12-5-2005